# DESIGN AND OPTIMIZATION OF MICROWAVE LUMPED ELEMENTS FILTERS USING MIXED CIRCUITAL-ELECTROMAGNETIC SIMULATIONS

**D. Neculoiu[*], A.A. Muller[**], F. Giacomozzi[***], D. Vasilache[*], I. Petrini[*], C. Buiculescu[*], A. Muller[*]**

[*]IMT-Bucharest, Erou Iancu Nicolae str. 32 B, 077190 Bucharest Romania
[**]Technische Universitaet Muenchen, Arcisstr. 21, D-80333 Muenchen, Germany
[***]ITC-IRST, Via Sommarive 18, 38050 Povo Trento, Italy

**Abstract–**_This paper presents the design, fabrication and experimental results of the switchable band-pass lumped elements filters. The design is based on a new optimization approach that integrates mixed circuital and electromagnetic simulations. The use of horizontal internal ports and the connection of external capacitors at circuital level make the optimization procedure very efficient. A very good agreement between measurements and simulations validate the new design approach._

## 1. INTRODUCTION

The wireless communication applications need RF transceivers operating in multiple separated frequency bands such that users can access various services with a single terminal. For this application RF dual-band selection filters are needed [1]. The conventional approach uses separate band-pass filters for each band and switches for frequency band selection.

Planar lumped inductors and capacitors are used in microwave active and passive integrated circuits. Unfortunately, the operation of these components at frequencies close to 5 GHz is limited by their intrinsic resonant frequency. In the case of planar inductors one solution consists in using micromachining technologies to remove the bulk substrate under the structure, resulting in decreasing the parasitic capacitance and increasing the resonant frequency [2, 3].

One solution to fabricate very compact switchable band-pass filters is to insert the RF MEMS switches into the LC filter layout [4]. The filters include resistive switches for the selection of DCS1800 and WLAN standards. Some spiral inductors and interdigital capacitors (IDC) are supported on a thin dielectric membrane fabricated using high resistivity silicon micromachining.

The design and optimization of lumped elements filters is not an easy task. Because the filters' specifications cover the frequency range up to 10 GHz, the classical analytical or circuital models are no longer accurate intensive electromagnetic (EM) simulations must be used in filter design. On the other hand, the high values required by the IDC capacitances necessitate three dimensional EM modeling for the digits metallization. These result in a very inefficient design of the filters layout when using optimization procedures.

This paper presents the design, fabrication and measured results of the switchable band-pass lumped elements filters for the DCS1800 and WLAN frequency ranges. The design is based on a new optimization approach that integrates mixed circuital and electromagnetic simulations. First, the fabrication of the filters is briefly described. Next, the design approach, the interdigital capacitors model and the optimization procedure is explained in detail. The last section presents the microwave measurement results and the comparison with the simulations.

## 2. FABRICATION

In order to obtain the filter structures having suspended air bridges on membranes, high resistivity p type <100> oriented silicon wafers have been used. A technological process with two distinct steps was developed [5]. First, the well known process of manufacturing the three layers $SiO_2/Si_3N_4/SiO_2$ membrane has been performed [6]. The thickness of the layers was calculated in order to compensate the stress in the membrane. The filters structures were defined using 6 μm of AZ4562 photoresist. Then 2.5μm of gold was selectively grown by electroplating in the resist-free windows. The air bridges were obtained by depositing first a sacrificial layer constituted by 2μm thick photoresist (baked 1 hour at 200°C) and then selectively depositing over it, by

electroplating, a second 2.5µm thick gold layer.

The second step of the process consisted in the tricky way to release the air-bridges (by surface micromachining) as well as the membranes (by bulk micromachining). The front side was first covered by 4.5 µm of a protective polymer (AR-PC 504), the backside silicon was removed by anisotropic etching and finally both the protective polymer and the sacrificial resist have been removed by oxygen plasma.

An optical photo of the fabricated membrane-supported spiral inductor with membrane-supported air-bridges is presented in Fig. 1. The strip width and the separation between two inductor's strips are 50 µm. Air-bridges are used to equalize the potentials of the ground metallization. Fig. 2 shows the optical photo two membrane-supported IDCs. The digit width is 40 µm and the gap between two digits is 10 µm. A detail of the IDC is presented in the SEM photo from Fig. 3.
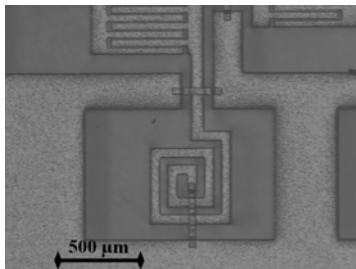


**Fig. 1.** Optical photo of the membrane-supported spiral inductor.
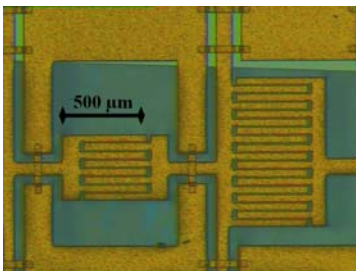


**Fig. 2.** Optical photo of two membrane-supported interdigital capacitors.

## 3. FILTERS DESIGN

### 3.1. The Design Approach

The topology of the tunable band-pass filter is similar with that presented in Fig. 4 [4]. In order to obtain a very compact layout the RF MEMS series resistive switches (used to change the LC components values) are inserted into the filter structures. The spiral inductors are chosen to be the same for both DCS1800 and WLAN frequency bandwidths. The spiral inductors and part of the interdigital capacitors are supported on a thin dielectric membrane fabricated using high resistivity silicon micromachining.

The tunable band-pass filter structures are fabricated in coplanar waveguide (CPW) technology. The main steps of the design procedure are as follows [4, 5]:

**1.** Intensive electromagnetic (EM) simulations of different lumped components and database creation.

**2.** Filter prototype design using the Ansoft Designer SV software package. This software permits the design of low-pass, high-pass, band-pass and band-stop filters in an interactive and intuitive manner, using lumped and/or distributed components. The design consists of a trade between the filter frequency response shapes and the available component values from the database.

**3.** Filter layout generation and preliminary EM analyses with Zeland IE3D software package [7]. Because of the frequency dispersion of the lumped components parameters, the results differ from the prototype frequency response.

**4.** Layout optimization starting with the results from step 3 as the initial guess.
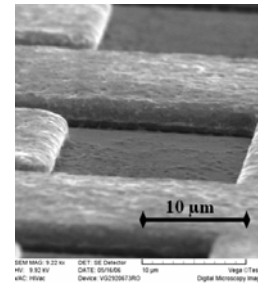


**Fig. 3.** SEM photo of the interdigital capacitor (detail).
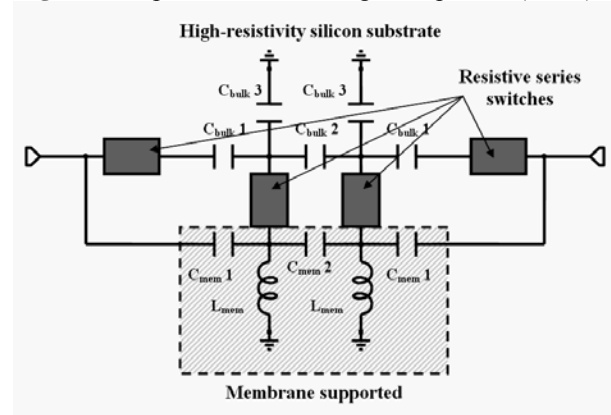


**Fig. 4.** The topology of the tunable band-pass filter with RF MEMS resistive switches.

The IE3D is a full-wave, method-of-moments based electromagnetic simulator solving the current distribution on 3D and multilayer structures of general shape. The IE3D software includes an optimisation engine that allows the definition of multiple objective functions. The optimised independent variables are the layout dimensions.

## 3.2. The Interdigital Capacitor Model

As it can be noticed in Fig.3, the 2.5 μm thickness of the gold layer is comparable with the 10 μm separation between two digits. In this case, the standard infinitely thin strip model of IE3D will cause very poor accuracy in the EM simulations. The IE3D features the "Thick Strip Model", a more sophisticated scheme that includes the current flowing on the 4 surfaces of the strip (see the inset in Fig.5). This model matches the physics very well, but increases a lot the simulation time and the computer memory requirement. Both are very important in an efficient design based on optimization procedures.

In order to solve this problem, a new mixed circuital-electromagnetic optimization approach was developed. For every IDC of the filter a horizontal internal port was added, as shown in Fig.5. The EM simulation are performed using "Thick Strip Model" and the results are saved into *.sNp Touchstone type data files. At circuital level, an external capacitor ΔC is added for every IDC, as shown in Fig.6. The external capacitor is placed in parallel and its capacitance is added to the IDT capacitance obtained by means of EM simulations.
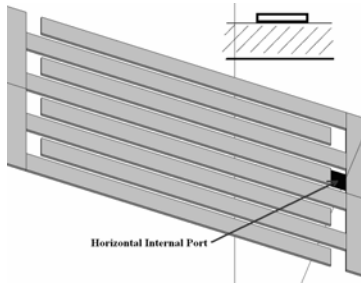


**Fig. 5.** The interdigital capacitor "Thick Strip" EM model and the horizontal internal port position.
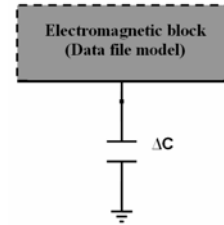
## 3.3. Optimization Procedure

Using the IDT modeling approach described in the previous section, the filter design and optimization is shifted from the electromagnetic simulation level to circuit simulation level. As a result the optimization speed is increased with several orders of magnitude without losing analyses accuracy.

The optimization started from step 4 of the design described in section 3.1. The new independent variables vector is defined as:

$$\mathbf{X} = \left\{ \Delta C_{mem1}; \Delta C_{mem2}; \Delta C_{bulk,1}; \Delta C_{bulk,2}; \Delta C_{bulk3} \right\} \quad (1)$$

where $\Delta C_{mem,k}$ and $\Delta C_{bulk,k}$ represent the amount of capacitance that is added (or subtracted) to the values obtained using EM simulations (see also Fig.4).



**Fig. 6.** Detail of the equivalent circuit with external capacitor added to the EM model.

The objective (error) function $F$ of the optimization process is defined in (2). First, the optimization was performed for the WLAN frequency range using the first two variables defined in (1). The EM simulations were performed with the RF MEMS switched in the UP state. After, the last three variables from (1) were used to fulfill the DCS1800 filter specifications. The EM simulations of the filter layout were performed with the RF MEMS switched in the DOWN state. Finally, all 5 variables were changed and the filter performances were fine tuned to the full frequency range desired response.
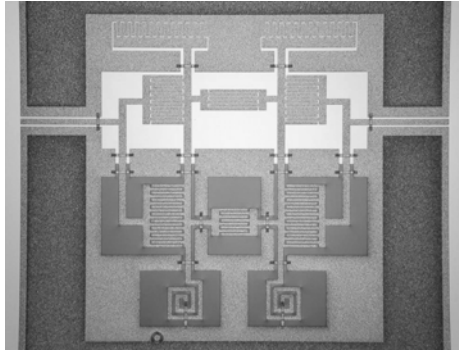
$$F(\mathbf{X}) = \sum_{freq} \left[ S(\mathbf{X}, freq) - D(freq) \right]^2 \quad (2)$$

where: $freq$ is the frequency range, $S$ represents the simulated filter response (S parameters) and $D$ is the desired filter response.

Very important for an efficient design is to update the length of the IDC digits after every successful optimization. The IDC sensitivities were estimated using EM simulations and the obtained values are presented in Table 1.

**Table 1.** Interdigital capacitor sensitivities

| Capacitor | No. of digit pairs | Sensitivity [fF/ μm] |
|---|---|---|
| $C_{mem,1}$ | 9 | 0.33 |
| $C_{mem,2}$ | 4 | 0.14 |
| $C_{bulk,1}$ | 7 | 0.83 |
| $C_{bulk,2}$ | 3 | 0.347 |
| $C_{bulk,3}$ | 12 | 0.034 |

**Fig. 7.** The photo of a filter structure for DOWN state.



**Fig. 8.** a Simulated (solid line) and experimental (squares) responses for the filter with ideal switches in DOWN state.



**Fig. 8.** b Detail of the simulated (solid line) and experimental (squares) responses for the filter with ideal switches in DOWN state.
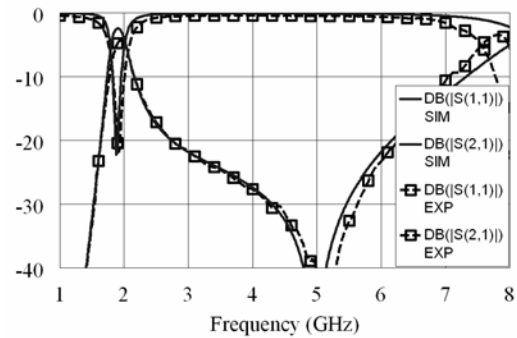
## 4. MEASUREMENTS

In order to test the new optimization approach, the RF MEMS switches were modeled with ideal resistive contacts in the DOWN state and open circuits in the UP state. Several wafers with filters test structures with ideal resistive switches in both UP and DOWN states were fabricated. The photo of a filter structure for DOWN state is presented in Fig.7.

The filter structures S parameters were measured in the 1-8 GHz frequency range, using the Vectorial Network Analyzer Anritsu 37397D and the "on wafer" measurement system Suss MicroTec equipped with Picoprobe probes.
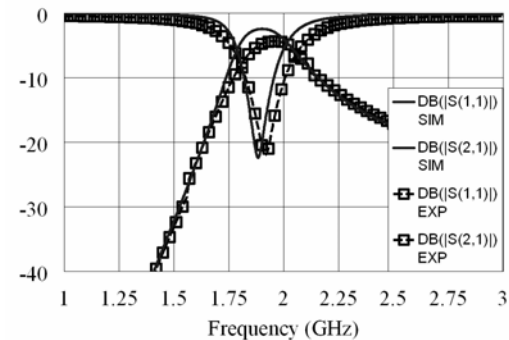
A comparison between the measured and simulated results for the filter with ideal resistive switches in DOWN state is presented in Fig.8.a (full range) and Fig.8.b (detail). The agreement is good, but there is a small shift in the central frequency of about 34 MHz and the measured losses are 1.8 dB higher than the simulated ones.

## 5. CONCLUSIONS

The design, fabrication and experimental results of the switchable band-pass lumped elements filters were presented. The design is based on a new optimization approach that integrates mixed circuital and electromagnetic simulations. The "Thick Strip" model was use for the accurate IDC modelling. The use of horizontal internal port feature of the EM software and the connection of external capacitors at circuital level make the optimization procedure very efficient. A very good agreement between measurements and simulations validate the new design approach.

**References**

[1] M. Golio, "The RF and Microwave Handbook", *CRC Press LLC*, 2001.

[2] Gabriel M. Rebeiz, "RF Mems Theory ,Design and Technology", J*ohn Wiley & Sons*, 2003.

[3] C.Y. Chi, G.M. Rebeiz, "Planar Microwave and Millimeter-Wave Lumped Elements and Coupled-Line Filters Using Micro-Machining Techniques", *IEEE Trans. On MTT*, vol. **43**(4), 1995, pp. 730-736.

[4] D. Neculoiu, F. Giacomozzi, L. Bary, D. Vasilache, A.A. Muller, B. Margesin, I. Petrini, C. Buiculescu, A. Takacs, R. Plana, A. Muller, "Compact lumped elements micromachined band-pass filters with discrete switching for 1.8/5.2 GHz applications", *Proc of CAS 2006*, pp. 107-110.

[5] F.Giacomozzi et al, "Surface and Bulk Micromachining for Lumped Components Filters Manufacturing", *MEMSWAVE 2005– Digest of Technical Papers*, Lausanne, Switzerland, 2005, pp.169-172.

[6] N. Dib, W. Harokopous, L. Katehi, "Study of a novel planar transmission line", I*EEE MTT-S*, 1991, pp.623-6.

[7] *IE3D User's Manual*, Zeland Software Inc., Freemont, CA, www.zeland.com.